Docket No.: FISCHBACH-6
Appl. No.: 10/700,351

AMENDMENTS TO THE SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Amend the title to read: --HIGH DATA RATE ACTUATOR/SENSOR CONTROL SYSTEM FOR A PLASTICS PROCESSING MACHINE--

Amend the following paragraph(s):

[0008] --European Pat. No. EP 0 917 034 describes a method for remote monitoring and/or remote maintenance of an injection molding machine. The injection molding machine is provided with a Programmable Logic Controller (SPS) ~~SPS~~ with at least one CPU for controlling the actuators of the injection molding machine in ~~real-time~~ real time. Data ~~are~~ is transmitted between the injection molding machine and a remote monitoring station located at a distal location for remote monitoring and/or remote maintenance. As described in EP 0 917 034, several actuators and sensors are connected via inputs and outputs to a real-time controller. The inputs and outputs can include a digital card or an analog card. However, EP 0 917 034 does not disclose that these cards are provided with pre-processing units. Accordingly, the inputs and outputs represent conventional interfaces which for high data transmission rates require an increased communnication bandwidth over a real-time-capable bus ~~systems~~ system.--.

[0022] --Turning now to the drawing, and in particular to FIG. 1, there is shown a CPU 4 which, as described in more detail below, is connected via a serial bus system 3 to an ASIC/FPGA unit 2. The ASIC/FPGA unit 2 includes a field programmable gate array (FPGA) and/or an application-specific integrated circuit (ASIC), which is specifically tailored to the present embodiment and the connected sensors or actuators. The ASIC/FPGA unit 2 is connected with at least one sensor and/or actuator 1 and preprocesses the signals received from the sensor and/or actuator 1. At least one sensor or actuator is implemented as

a component which can measure a rapidly fluctuating variable with high resolution. For example, the ~~The~~ resolution can be~~, for example~~ in the range of 16, 21 or more bits. These variable quantities are typically mechanical quantities, such as pressure, linear dimensions, total mass flow or similar quantities. However, some sensors - for example, the sensor unit or actuator unit 1' in FIG. 1 - can be directly connected with the serial bus system 3. In particular, ~~Suitable are here particular~~ those components which require only insignificant bandwidth resources from the serial bus system and whose data cannot be or need not be locally processed are suitable to ~~Such sensors or actuators can~~ be directly connected with the CPU 4 via the serial bus system.--

[0025] --It will be understood that several pre-processing units 20 can be connected to the serial bus system 16~~. Only~~, although only one pre-processing unit is depicted in FIG. 2. In addition, an input/output system (I/O system) 22 with analog inputs and outputs (AI, AO) and digital inputs and outputs (DI, DO) can be provided. --.

[0026] --The additional embodiment depicted in FIG. 3 differs from the embodiment depicted in FIG. 2 with respect to two details~~. Instead~~: 1) instead of the second pre-processing unit 18, a second CPU unit 24 (CPU 2) is provided downstream of ~~the~~ 2) a second bus system 16', which is implemented as a Small Computer System Interface (SCSI) ~~SCSI~~ bus. The first CPU unit (CPU 1) with the reference numeral 10' is connected with the second CPU unit 24 directly via the serial bus 16'. This "2-CPU controller" reduces the bus communication in particular through the use of the second CPU unit 24, which transmits to the first CPU unit 10' and receives from the first CPU unit 10' via the serial bus 16' only the signals required for the actual control.--.

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AMENDMENTS TO THE CLAIMS WITH MARKINGS TO SHOW CHANGES MADE, AND LISTING OF ALL CLAIMS WITH PROPER IDENTIFIERS

1. (Currently amended) A control system for a plastics processing machine, comprising:

a central processing unit adapted to execute ~~executing~~ a real time operating system;

a plurality of actuators and/or sensors connected via a bus system to the central processing unit, ~~with~~ at least one actuator and/or at least one sensor being directed to a rapidly fluctuating variable with a high resolution; and

at least one first pre-processing unit having at least one ASIC or FPGA, ~~wherein the plurality of actuators and/or sensors, of which~~ at least one actuator and/or sensor ~~is~~ directed to a rapidly fluctuating variable with a high resolution~~, is~~ being connected with the first pre-processing unit, ~~and wherein~~ the first pre-processing unit ~~is~~ being connected with the central processing unit via the bus system.

2. (Original) The control system of claim 1, and further comprising a second processing unit having a CPU and disposed between the bus system and the first pre-processing unit.

3. (Original) The control system of claim 1, and further comprising an I/O system directly disposed on the bus system.

4. (Currently amended) The control system of claim 2, ~~and~~ further comprising an I/O sytem disposed on the ~~second processing unit~~ bus system downstream of the ~~bus system~~ second processing unit.

5. (Original) The control system of claim 1, wherein the at least one first pre-processing unit is adapted to preprocess signals and match drivers for the sensors and/or the actuators, and to calibrate the sensors and/or the actuators.

6. (Original) The control system of claim 1, wherein the bus system is implemented as a serial bus.

7. (Original) The control system of claim 1, wherein the central processing unit includes an input device and a monitor.

8. (Original) The control system of claim 7, wherein the input device is a keyboard.

9. (Currently amended) The control system of claim 1,wherein at least one ~~first~~ pre-processing unit is configued to relieve the central processing unit from communicating via the bus.

10. (Original) The control system of claim 2, wherein the second pre-processing unit is configured to relieve the central processing unit from communicating via the bus.

11. (Currently amended) A control system for a plastics processing machine, comprising:

a central processing unit <u>adapted to execute</u> ~~executing~~ a real time operating system;

a plurality of actuators and/or sensors connected via a bus system to the central processing unit, ~~with~~ at least one actuator and/or at least one sensor being directed to a rapidly fluctuating variable with a high resolution; and

at least one pre-processing unit having at least one ASIC or FPGA arranged between the bus system and the central processing unit.

12. (Original) The control system of claim 11, wherein the bus system is implemented as a serial bus.

13. (Original) The control system of claim 11, wherein the central processing unit includes an input device and a monitor.

14. (Original) The control system of claim 13, wherein the input device is a keyboard.

15. (Currently amended) The control system of claim 11,wherein the pre-processing unit and/or ~~the other~~ another pre-processing unit are configued to relieve the central processing unit from communicating via the bus.

16. (Currently amended) A control system for a plastics processing machine, comprising:

a central processing unit adapted to execute ~~executing~~ a real time operating system;

a plurality of actuators and/or sensors connected via a bus system to the central processing unit, ~~with~~ at least one actuator and/or at least one sensor being directed to a rapidly fluctuating variable with a high resolution;

at least one first pre-processing unit having at least one ASIC or FPGA and connected with the central processing unit via the bus system; and

a second pre-processing unit having at least one ASIC or FPGA and disposed between the bus system and the central processing unit, ~~wherein the plurality of actuators and/or sensors, of which~~ at least one actuator and/or sensor ~~is~~ directed to a rapidly fluctuating variable with high resolution~~, is~~ being connected with the first pre-processing unit, ~~and wherein~~

the first pre-processing unit ~~is~~ being connected with the first pre-processing unit.

17. (Currently amended) A control system for a plastics processing machine, comprising:

a central processing unit adapted to execute ~~executing~~ a real time operating system[[,]];

a first operating element responsive to a fluctuating variable with a high resolution and operatively connected to the central processing unit via a bus system; and

a first pre-processing unit having at least one ASIC or FPGA and ~~disposed in~~ connected to the bus system between the central processing unit and the first operating element for locally processing the first operating element.

18. (Original) The control system of claim 17,wherein the operating element is a member selected from the group consisting of actuator and sensor.

19. (Original) The control system of claim 17, and further comprising a second said operating element connected to the bus system.

20. (Original) The control system of claim 17, and further comprising a second said pre-processing unit disposed on the bus system between the central processing unit and the first pre-processing unit.

21. (Original) The control system of claim 17, and further comprising an I/O system directly disposed on the bus system.

22. (Currently amended) The control system of claim 17, ~~and~~ further comprising a further central processing unit operatively connected to the ~~first~~ central processing unit via a second bus system, and an I/O system disposed on ~~the second bus pre-processing unit~~ a bus system downstream of the ~~bus system~~ further processing unit.

23. (Original) The control system of claim 17, wherein the bus system is implemented as a serial bus.

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AMENDMENTS TO THE DRAWINGS WITHOUT MARKINGS

IN THE DRAWING:

Fig. 1 has been amended.

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REMARKS

The last Office Action of June 22, 2005 has been carefully considered. Reconsideration of the instant application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-23 are pending in the application. Claims 1, 4, 9, 11, 15, 16, 17 and 22 have been amended. Amendments to the specification have been made.

It is noted that the Title has been rejected for not being descriptive. A new Title is submitted with this Response.

The objection to the specification has been addressed by amending paragraphs [0008] and [0026] of the specification. In response to the objection to the abbreviations "SPS" and "SCSI", paragraph [0026] has been amended to explicitly recite the well-known data communication term "SCSI" has been as Small Computer System Interface. Similarly, the term "SPS" on page 3 is in the description of the structures disclosed in European Pat. No. EP 0 917 034. Thus, the assertion that "SPS" is a term introduced by applicant is erroneous, and "SPS" must be interpreted by the reader in the context of that European patent disclosure, where in paragraph [0003] "SPS" is identified as "Speicherprogrammierbare Steuerungen bzw. PLC" that is, Programmable Logic Control. Paragraph [0008] has been amended accordingly.

In response to the objection to the drawings under 37 CFR §1.84(p)(5), call outs 1' and 1, indicating actuator units that obviously are and are not connected directly with the serial bus system 3, respectively, have been added to Fig. 1.

The objection to the drawings under 37 CFR §1.83(a) is hereby respectfully traversed. The assertion that Claims 1, 16, and 17 recite that actuators/sensors or operating elements are "connected to both" the bus system and a preprocessing unit is erroneous. Instead, Claim 17 as filed accurately recites that a first operating element is connected to the central processing unit via a bus system and that a pre-processing unit is disposed in the bus system

between the central processing unit and the first operating element. Similarly, Claims 1 and 16 as filed accurately recite a plurality of sensors/actuators "connected to the central processing unit via a bus system" (or "connected via a bus system to the central processing unit" which is equivalent) and a first pre-processing unit "connected with the central processing unit via the bus system". On the other hand, at least one of the plurality of sensors/actuators is directed to a rapidly fluctuating variable and is "connected with the first pre-processing unit" and so only "some" components of the plurality may be "connected with the first pre-processing unit".

Thus, pluralities of components that are operating elements or sensors/actuators that are connected to a respective bus system 3 or 16 are disclosed in each of the preferred embodiments described in paragraphs [0022], [0024 and [0026] in this application, and in accordance with the claimed invention at least "some" of the components in those pluralities of components are connected to a first pre-processor.

The rejection of claims 1-10 and 17-23 as filed, under 35 U.S.C. §112, first paragraph, as failiing to provide the required written description is hereby respectfully traversed.

As noted above with regard to the objection to the drawings under 37 CFR §1.83(a), the assertion that Claims 1 and 16 recite that actuators/sensors or operating elements are "connected to both" the bus system and a preprocessing unit is erroneous. Claims 1 and 16 as filed recite a plurality of sensors/actuators either "connected to the central processing unit via a bus system" (which is the same as "connected via a bus system to the central processing unit") and at least one sensors/actuators that is directed to a rapidly fluctuating variable being "connected with the first pre-processing unit", the first pre-processing unit being "connected with the central processing unit via the bus system." This is shown in the drawings where respective pluralities of sensors/actuators are connected to the respective bus system 3 or 16, respectively, as shown in FIG. 1 and described in paragraph [0022], either directly as is the component 1' or indirectly

through a preprocessor 2 as is the component 1'. Specifically, Fig. 1 shows a plurality of sensor/actuator devices all of which are connected to the CPU by a serial bus system 3. Some that have "high resolution" as defined in paragraph [0022] lines 8-12 are indirectly connected to the CPU through a pre-processor unit 2. However, one component 1' of this "plurality" is connected directly to the serial bus without being connected to a pre-processor, as explained in paragraph [0022] lines 8 -12.

In Figs. 2 and 3 the plurality of sensor/actuator components S_1 - S_n are all directly connected with the first pre-processor unit 20. In accordance with the claimed invention at least one such component is "always" a sensor/actuator "directed to a rapidly fluctuating variable" as recited in claims 1 and 16 as filed or an operating element "responsive to a fluctuating variable with high resolution" as recited in claim 17 as filed, which may be an actuator/sensor as recited in Claim 18 as filed, as is supported for FIG. 2 in paragraph [0023] at lines 5-6 and [0024] at lines 10-14, and confirmed for FIG. 3 in paragraph [0026] at lines 1-6.

Paragraph [0024] at lines 8-15 emphasizes that in FIG. 2 "several sensors or actuators S_1 to S_n are always connected to the first pre-processor" and at least one of these sensors/actuators is directed to a "rapidly fluctuating mechanical quantity, such as a pressure signal, a distance signal, a volume flow signal, etc." that produces a high resolution signal that would tax the capacity of the central processing unit if a corresponding pre-processing unit were not connected upstream, as further explained in paragraph [0023] at lines 5-9 with respect to FIG. 2, and with respect to FIG. 3 in paragraph [0026] at lines 6-9 and in paragraph [0027].

Furthermore, Claim 17 as filed recites that an operating element is "connected to the central processing unit via a bus system" and that a pre-processing unit is "disposed in the bus system between the central processing unit and an operating unit". As noted above with regard to the objection to the drawings under 37 CFR §1.83(a), the assertion that Claim 17 recites that actuators/sensors or operating elements are "connected to both" the bus system

and a preprocessing unit is erroneous.

In response to the rejection of claims 1-17 35 U.S.C. §112, second paragraph, as indefinite is hereby respectfully traversed.

"ASIC" and "FPGA" are explicitly defined in paragraphs [0004] and [0009] of the specification as filed. The elements of the Claims are interpreted in the light of the disclosure provided by the specification.

The recitation in Claim 17 of a first pre-processor "disposed in" the bus system in claim 17 has been amended to "connected to the bus system " is supported by the specification in paragraph [0025] at lines 1-2.

The recitation of "high resolution" is supported by the specification in paragraph [0022] with reference to FIG. 1, and in paragraphs [0023], [0026] and [0027] with reference to FIGs 2 and 3, as noted above with reference to the rejection of claims 1-10 and 17-23 as filed, under 35 U.S.C. §112, first paragraph.

In paragraph [0003] of the Background of the Invention, applicants point out that the problem addressed by applicant's invention arises from the increased bus system bandwidth required by digital sensor and actuator instrumentation for their complex identification, calibration and adaptation protocols. In particular, improvements in the cost-efficiency of serial bus systems has not kept pace with this change, laging behind the simultaneous improvements in CPU capacity. Furthermore, although the bus system is currently the bottleneck in designs for real-time control of plastics processing machines, in particular, eliminating that bottleneck by providing separate CPU/RAM control facilities configured to accomodate respective different types of sensor and/or actuator protocols is "economically difficult".

In particular, of the plurality of operational elements shown in FIG. 1, some operational elements 1 have "high resolution" as defined in paragraph [0022] lines 8-12:

> *At least one sensor or actuator is implemented as a component which can measure a rapidly fluctuating variable with high resolution. For example,*

the resolution can be in the range of 16, 21 or more bits. These variable quantities are typically mechanical quantities, such as pressure, linear dimensions, total mass flow or similar quantities.

As explained in paragraph [0023] at lines 5-9 and [0024] at lines 10-14 with respect to FIG. 2, and in paragraph [0026] at lines 6-9 and in paragraph [0027] with respect to FIG. 3, among the plurality of sensors/actuators S_1 to S_n at least one of them is an element that produces a "high resolution" signal that would tax the capacity of the central processing unit if a corresponding pre-processing unit were not connected upstream. Once again the examples given are a "pressure signal, a distance signal, a volume flow signal, etc." for a plastics processing machine.

The recitation in Claim 4 as filed of "downstream" of a bus system is supported by the specification in paragraph [0026] and FIG. 3, in which the second CPU is provided on the downstream end of the second bus system 16' that connects the two CPUs 10' and 24. Claim 4 has been amended to recite that the I/O sytem is on a bus system downstream from the second processing unit, which is consistent with the desciption provided in paragraph [0026] and the I/O system shown in FIG. 3 wherein the I/O system is downstream from the second processing unit on another bus system, one that is analogous to the first bus system 16, as confirmed in paragraph [0026].

The recitation in Claim 9 as filed that a pre-processing unit is configured to "relieve the central processing unit from communicating via the bus" is supported by the specification in paragraph [0023] lines 3-5. Claim 4 has been amended for the sake of providing a recitation clearly consistent with this disclosure. In paragraph [0023] applicant points out that the wait cycles required for receiving a bus response do not adversely affect the availability of the CPU for control computation if a preprocessor communicates information to the CPU instead of the bus, as recited in Claims 9, 10 and 15.

In Claim 10, base Claim 2 recites "a second processing unit" providing clear antecedent basis for "the second processing unit" recited in Claim 10. In

paragraph [0023] applicant points out that the wait cycles required for receiving a bus response do not adversely affect the availability of the CPU for control computation if a preprocessor communicates information to the CPU instead of the bus, as recited in Claims 9, 10 and 15.

In Claim 15, base Claim 11 recites "a processing unit" and Claim 11 has been ameded to recite "another pre-processing unit" as shown in FIG. 2 and described in paragraph [0023] . In paragraph [0023] applicant points out that the wait cycles required for receiving a bus response do not adversely affect the availability of the CPU for control computation if a preprocessor communicates

The rejection of claim 20 is hereby respectfully traversed as erroneous. There reference to "downstream" etc. is in Claim 22, not Claim 20. In Claim 22 as filed the recitation of "downstream" on a bus system is supported by the specification in paragraph [0026] in which the second CPU is connected to the downstream end of a second bus system 16' that connects the two CPUs 10' and 24 and and by FIG. 3, which shows that the I/O system is downstream of the second CPU on another bus system, one that is analogous to the first bus system 16, as noted above with reference to claim 4. Claim 22 has been amended to recite that the I/O sytem is on a bus system downstream from the second processing unit, which is consistent with the desciption provided in paragraph [0026] and shown in FIG. 3 .

Minor editorial changes made for the sake of clarity, consistent terminology, in addition to the changes discussed above, are provided herein.

Applicant notes with appreciation that claims 18-23 have been found to be patentable over the prior art cited.

The rejection of claims 1-4 and 6-7 under 35 U.S.C. § 102(e) as anticipated by Moon et al. is hereby respectfully traversed.

Claim 1 recites at least one ASIC or FPGA connected to at least one sensor/actuator that is responsive to a rapidly fluctuating varible with a high resolution. Moon discloses a field bus controller 320 that controls a buffer memory 320, decodes data, stores and communicates data to a main controller

310, which communicates with a computer 20 to prevent duplication of effort between the field bus controller and the microcontroller attaced to it. There is no rapidly fluctuating varible and no no bus system having an ASIC or FPGA and no sensor/actuator that is disclosed as responsive to a rapidly fluctuating varible with a high resolution.

The rejection of claims 1-4 and 6-7 under 35 U.S.C. § 102(b) as anticipated by Bermann et al. is hereby respectfully traversed.

Claim 1 recites at least one ASIC or FPGA connected to at least one sensor/actuator that is responsive to rapidly fluctuating varible with a high resolution. Bermann discloses a monitoring unit that allegedly relieves its PC processor of polling process data and monitoring a field bus, so as to make it transferable to a new system without major changes, col. 2, lines 18-27. Alternatively, this transferability can be implemented by reprogramming a communications processor 14 in the computer, col. 2, lines 27-29. Again, there is no rapidly fluctuating varible and no bus system having an ASIC or FPGA and no sensor/actuator that is disclosed as responsive to a rapidly fluctuating varible with a high resolution.

The rejection of claims 1-17 under 35 U.S.C. § 102(b) as anticipated by Goetze et al. is hereby respectfully traversed. Claims 1, 11, 16 and 17 recite at least one ASIC or FPGA and at least one sensor/actuator that is responsive to rapidly fluctuating varible with a high resolution. Goetze discloses a heirarchical processor architecture having two processor levels, wherein a processor 1 again provides adaptatabilty for a computer to different control protocols, somewhat similar to Bermann.

Again in Goetze there is no rapidly fluctuating varible and no bus system having an ASIC or FPGA and no actuator/sensor disclosed as responsive to a rapidly fluctuating varible with a high resolution. In particular, there is no ASIC or FPGA arranged between the bus system and the central processing unit, and no no actuator/sensor disclosed as responsive to a rapidly fluctuating varible with a high resolution connected to pre-processing unit having the ASIC or FPGA, and

no ASIC or FPGA disposed in a bus system between the central processing unit and a first operating element responsive a fluctuating varible with a high resolution and operatively connected to the central processing unit via a bus system.

Applicant believes that the scope of the claims originally filed would have been allowable over the citations in this Office Action; therefore, no claims have been narrowed so as to trigger prosecution history estoppel. Claims have been amended for the sake of clarity, conformity to United States patent practice and consistency with the disclosure provided in this application. No new matter has been added.

In view of the above presented remarks and amendments, it is respectfully submitted that all claims on file should be considered patentably differentiated over the art and should be allowed.

Reconsideration and allowance of the present application are respectfully requested.

Should the Examiner consider necessary or desirable any formal changes anywhere in the specification, claims and/or drawing, then it is respectfully requested that such changes be made by Examiner's Amendment, if the Examiner feels this would facilitate passage of the case to issuance. If the Examiner feels that it might be helpful in advancing this case by calling the undersigned, applicant would greatly appreciate such a telephone interview.

Respectfully submitted,

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